Crystalline Silicon Interconnected Strips (XIS): Introduction to a New, Integrated Device and Module Concept

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***Abstract* — A new device concept for high efficiency, low cost, wafer based silicon solar cells is introduced. To significantly lower the costs of Si photovoltaics, high efficiencies and large reductions of metals and silicon costs are required. To enable this, the device architecture was adapted into low current devices by applying thin silicon strips, to which a special high efficiency back-contact heterojunction cell design was applied. Standard industrial production processes can be used for our fully integrated cell and module design, with a cost reduction potential below 0.5 €/Wp. First devices have been realized demonstrating the principle of a series connected back contact hybrid silicon heterojunction module concept.**

***Index Terms* — amorphous materials, back contact, heterojunction, photovoltaic cells, series connection, silicon.**

I. Introduction

In recent years, PV system prices have gone down rapidly, reaching grid parity levels in large parts of the world. Meanwhile industry faces competitive times and focus has been on market share. However, we still have a large task to increase efficiency in combination with lower costs to realize a true sustainable solution for large scale electricity generation. Materials supply chain security, price stability and possible scarcity will be important as well. Even with the use of earth abundant materials, the scale that is necessary to install terawatts of PV and the economics related to that force the minimization of materials consumption. To reach high efficiencies crystalline silicon wafer technology is one of the most important candidates because of the high material quality that can be reached in the purification process, which is already available at large scale production. The XIS concept (XIS stands for Crystalline Silicon (X) Interconnected Strips) combines the high efficiency of crystalline silicon wafer technology with a much reduced bill of materials and high throughput, such as large area processing as is possible with thin film PV technologies.

II. Description of the XIS Concept

To be able to reduce the amount of metal that is used in PV cells and modules, the current needs to be reduced, especially because Ag is an important cost factor in today's crystalline Si based PV modules. In the concept proposed here, this lower metal consumption is achieved by reduction of the cell size, e.g. dividing 156 x 156 mm^2 wafers into 52 strips of 3 mm width and connecting them in series. The reduction of the required amount of metal can almost go quadratic with the reduction of cell width, if full area metal coverage is used and the direction of current transport is in the direction of the width of the strips. We estimate that the required amount of metal can be reduced with a factor of 600 to 1000. This allows the use of very thin layers of metals or the use of less conductive, less expensive materials, even for instance carbon-based materials. In this way, low currents and high voltages are realized.

It is proposed that the individual strips are not handled separately, which is one of the differences with the well known Sliver concept [1], that also employs silicon strips. Before strip formation, the wafers are adhered to a superstrate. First, the front sides of the wafers are processed, e.g. texture, FSF, and passivation. Then, the wafers are bonded to the sun-receiving superstrate. In this way, only a minimum amount of process steps needs to be performed on wafer level, enabling the use of ultra-thin wafers (20-50 µm) and therefore reducing the costs of silicon, still the largest fraction of the materials costs. Conceptually, there are interesting similarities with the i-module approach [2]. In the XIS approach [3], after bonding, processing is done on module level, enabling high throughput: separation of the strips, junction and BSF formation, metallization and interconnection (isolation). Given the relatively small cell sizes, the edges of the cell will need to be well-passivated. After bonding the processing temperature is restricted to the maximum temperature tolerated by the (transparent) adhesive, e.g. around 200 °C in the case of silicones. Therefore, back contact heterojunction (BC-HJ) solar cells are used, see Fig. 1.

The cells as displayed in Fig. 1 have a heterojunction emitter consisting of an intrinsic amorphous silicon, a-Si:H(i), and p-type amorphous silicon, a-Si:H(p), extending over the largest part of the rear surface for efficient collection of minority carriers. The BSF is located at the edge of the rear surface. Majority carrier transport can be realized through bulk and front surface field (FSF). In this way a new concept for hybrid back contact silicon heterojunction solar cells is realized [3]. The front surface is arranged for optimal light coupling, e.g. by a random pyramid texture and passivating anti-reflection coating (ARC, not shown) and is laminated to the transparent superstrate (sunny side) with a transparent encapsulant. To isolate the cells from each other grooves are

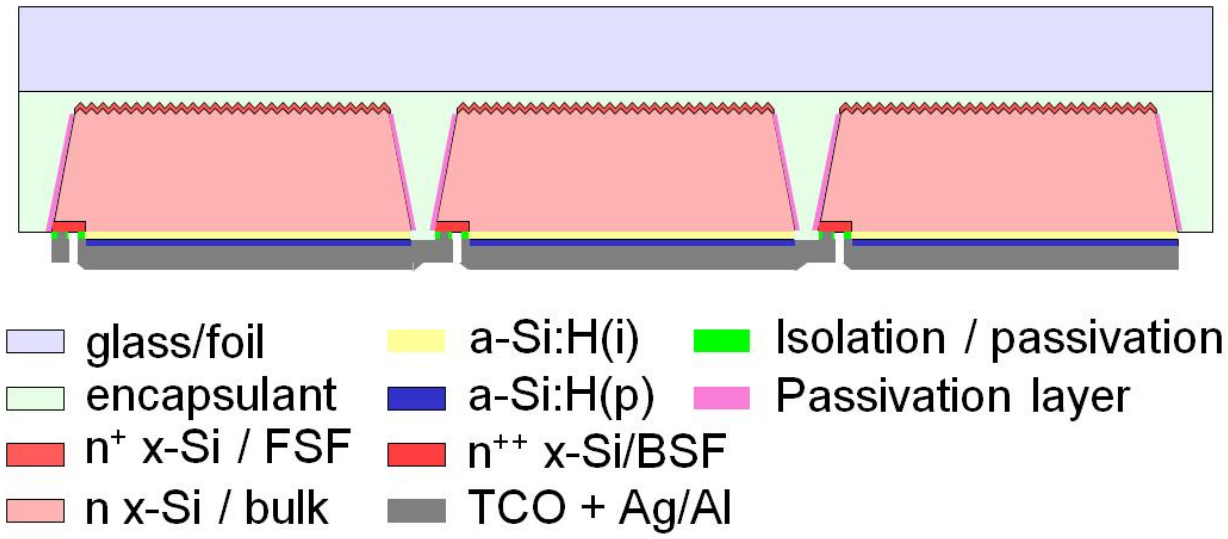

Fig. 1. Schematic cross section of a XIS module (not on scale) showing a series connection of three out of many strips. Individual cells / strips typically have a width of one to a few mm only.

made in the wafers. The sidewalls of the grooves are passivated. A metal and optional transparent conducting oxide (TCO) provide a series connection over the groove to the adjacent cell. Isolation between emitter and BSF contacts is arranged over the BSF area. The module can be completed with a backsheet foil or glass plate (not shown).

The schematic cross section as is shown in Fig. 1 and the integrated cell and module architectures that are described are examples of the possibilities to realize XIS devices. Other options include e.g. bonding to the rear substrate, different full back-contact heterojunction designs, like making use of an amorphous silicon BSF as well as emitter, several options for making grooves and their passivation, and contacting and isolation.

III. High Efficiency Back Contact Heterojunctions

Since the emitter formation of the solar cells is foreseen after bonding of the wafers to the glass superstrate, the options for emitter formation are more restricted than with standard solar cells. However, Si HJ solar cells have demonstrated to have an excellent efficiency potential. The highest efficiency reported to date is 23.7% [4] on an area of 100.7 cm^2. The XIS concept differs in several aspects from standard HJ devices, like those of Sanyo [4].

A. Back contact

In front junction heterojunction devices light absorption from the TCO and amorphous silicon layers slightly lower the efficiency. In addition, there is shading by the screen-printed metal pattern. In back-contact devices both are not present (at the front side). The efficiency potential for BC-HJ structures has been modeled by Das et al. [5] to be 24-26%. Sanyo is aiming for $\eta = 25\%$ laboratory devices [4]. Mingirulli et al. [6] have obtained an excellent $\eta = 20.2\%$ for a BC-HJ device, demonstrating for the first time that BC-HJ devices can also reach high efficiencies in practice. Recently, LG even published $\eta = 23.4\%$ employing photolithography and 20.7% with industrial processes on 156 x 156 mm^2 wafers [7].

B. Thin wafers

The aim of the XIS concept is to enable the use of thin wafers, e.g. with 20-50 µm thickness (with excellent light trapping), to reduce the Si material consumption. In itself, the concept is not restricted to thin wafers and high efficiencies can also be obtained with standard wafer thicknesses. Due to the excellent surface passivation, it can be expected that for heterojunction devices efficiencies do not decrease with decreasing wafer thickness. They might even slightly increase due to the higher voltage. In fact, the record efficiency obtained by Sanyo has been obtained with a 98 µm thick wafer, compared to the more than 200 µm thick wafer for the previous record of $\eta = 23.0\%$ [4].

C. Hybrid technology

For production purposes, it might be interesting to combine a heterojunction emitter with a diffused BSF rather than a hetero-BSF as is used in standard (IBC) heterojunction solar cells, due to more degrees of freedom with respect to masking and aligning. Both options are possible for the XIS concept.

IV. Materials Cost Reduction

The main purpose of XIS is to reduce the bill of materials. The bill of materials for PV modules can be assigned to three main functionalities: the photovoltaic effect, electrical

TABLE I
COMPARISON BETWEEN ESTIMATED MATERIALS CONTENT AND BILL OF MATERIALS FOR REFERENCE H-PATTERN/MWT MODULES AND XIS.

Material	Reference module		XIS	
	g/m^2	€/m^2	g/m^2	€/m^2
Si	1200	48.0	116	4.7
Cu	330	9.9	-	-
Ag	13	6.2	-	-
Al	70	5.8	2.7	0.2
Al-bussing	-	-	30	2.2

transport, and packaging, including weather protection and isolation. The main advantages of XIS are the reduction of the amount of metal required for electrical transport on the cells, from cell to cell and to the junction box and enabling the use of thin wafers, lowering the amount of silicon required.

In standard cells, Ag and Al screen printing pastes are used for metallization on the cells and copper tabs and bussing for interconnection between the cells and to the junction box. Due to the high currents up to 9 A for the 156 x 156 mm^2 large wafers, large amounts of metals are used in order to reduce series resistance and FF losses on cell and module level. By reducing the cell width to only a few mm and organizing the transport direction perpendicular to the cell width, less than a µm of metal is necessary to transport the power from cell to cell. It is assumed that series connection can be achieved with sputtered Al. In this way, a high voltage is built up, which also contributes to a reduction of the amount of metal that is necessary for the bussing to connect the wafers to the junction box. Furthermore, no expensive Ag is needed anymore! Combinations of series and parallel connections allow to regulate the module voltage.

The amount of silicon that is necessary for present-day modules is estimated at about 6 g/Wp, although a large part of which does not end up in the module. For the XIS potential calculation, it is assumed that the wafer thickness is 50 µm (although perhaps even 20 µm is possible in the future) and that there are no kerf losses or other losses. This is an idealized situation. The silicon price is chosen at 40 €/kg. Several approaches to realize thin wafers, reduction of kerf-loss and kerf-free wafering are under development at various companies and institutes. Amounts and prices of metals are estimated from a reference H-pattern / metal wrap through cell and module technology. In Table 1 a comparison between the rough data of the reference module and XIS is made. This delivers a rough estimates for the bill of materials. Processing costs are not included. It can clearly be seen both from the silicon aspect and from the metal consumption, XIS is an interesting way forward.

V. PRODUCIBILITY, REVOLUTION RATHER THAN EVOLUTION

Although the XIS concept appears to be quite different from standard silicon wafer technology, the development towards XIS can be regarded more as an evolution rather than a revolution. The main component that is added by XIS is the full module area processing. This is the long term application perspective, which is appealing for high throughput processing. After processing the wafers up to the front side, the wafers are transferred to the glass superstrate and from there on processed on the module level. These processes are already available in the thin film PV industry and the display technology. Laser processes for accurate interconnection and isolation on full module level are well known in most thin film PV technologies, including a-Si, CdTe and CIGS and large area laser micromachining with little damage is demonstrated e.g. in lens fabrication [8]. In thin film PV and display technology large area deposition of semiconductors with high accuracy has been developed already. In plasma display technology, screen printing on large areas, 2x2 m^2, with accuracies approaching 10 µm is industry practice [9].

The long term perspective of XIS is making full advantage of low silicon costs with thin wafers, low metals costs and high throughput processing. For the short term already the reduced metals costs are sufficiently interesting, especially since no or almost no silver needs to be used. Therefore, also with standard wafer thickness the application potential is interesting. In this case, all process steps are executed on wafer level, just as state-of-the-art technology, with standard equipment. The formation of the strips is done as the last step before module integration. Only passivation of the grooves needs to be done on module level, for which several options are available with existing large area equipment, e.g. PECVD.

VI. FIRST XIS DEMONSTRATION DEVICES

The future potential of the XIS technology makes use of thin silicon wafers that are laminated to the substrate as early as possible in the process flow to prevent handling of the extremely thin wafers as much as possible. To demonstrate the principle, however, we have used standard wafers with

standard thicknesses and have performed several processing steps on wafer level before laminating the devices to glass. Before starting the entire process flow, first several individual process steps were tested. Groove making was accomplished with a UV laser, multiple passes. In this way smooth and tapered grooves can be realized, see Fig. 2 (a).

To realize the first XIS demonstration devices, bonding of the strips to glass was accomplished with EVA. In first tests, EVA penetrated the grooves and was spread partly over the rear surface of the test structures, see Fig. 3 (left). By adjusting lamination pressure and groove width it was realized that the EVA mainly remains in the groove, see Fig. 3 (right).

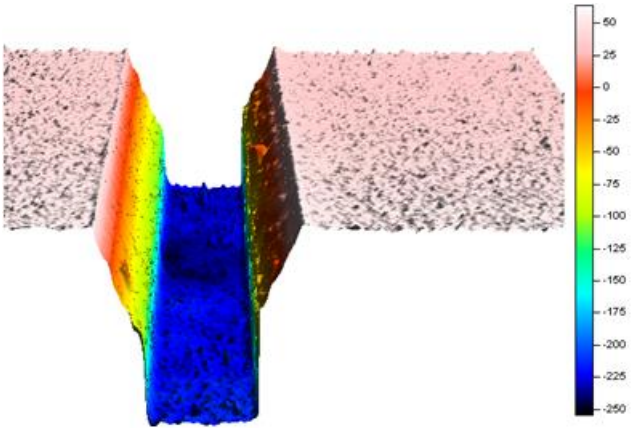

Fig. 2. Groove profile (µm) obtained with a scanning UV laser.

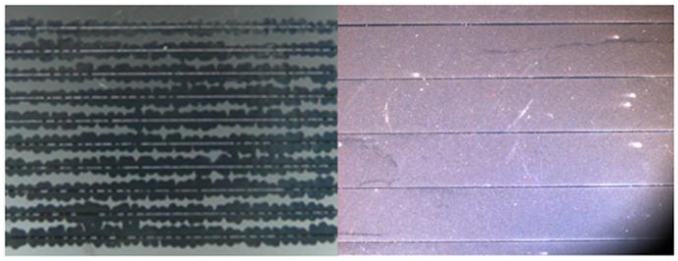

Fig. 3. Results of groove filling experiments. Left: EVA has flown over the rear surface. Right: EVA almost stays completely in the grooves.

The process sequence to realize the first XIS demonstrator mini-modules was: random pyramid texture; diffusions to realize FSF and BSF; 1st SiNx ARC pass half thickness; laser grooves and laser damage removal etch; 2nd SiNx ARC pass, realizing also groove passivation; amorphous silicon intrinsic and p-type doped layer deposition by PECVD; ITO sputtering; followed by lamination to glass with EVA and laser isolation and contacting and metallization. Three individual XIS mini-modules were processed from standard 156 x 156 mm^2 semi-square n-type Cz wafers, see Fig. 4 and Fig. 5. From the front side the laser grooves can be seen, indicating the areas where the mini-modules have been realized. Three different strip widths were used, 3.0 mm (top), 4.0 mm (middle), and 3.5 mm (bottom). Only after lamination to glass the strips were cut loose from the wafer by a laser.

After device preparation IV characteristics of the mini-modules were measured. The measurements demonstrate that a successful series connection of all ten cells in a mini-module has been achieved with a realized mini-module voltage of 2.6 V, measured between position 1 and 11 (see Fig. 5). Maximum individual cell voltage was 0.43 V. This is the first successful demonstration of XIS devices. It is an important result that all features of the XIS concept have proven to be functional, including the realization of a hybrid BC-HJ structure, groove formation, groove passivation, and series connection. However, the efficiency results that were achieved are not impressive with low currents, voltages and FFs, although the best pseudo-FF that was achieved was 76%.

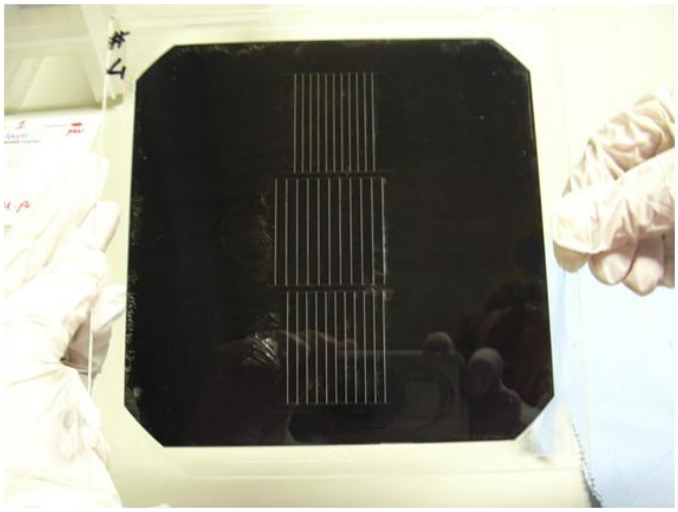

Fig. 4. Front (sunny) side of first realized XIS demonstrator mini-modules. Three mini-modules are realized in one wafer, with 3 mm strip width (top), 4 mm strip width (middle) and 3.5 mm strip width (bottom).

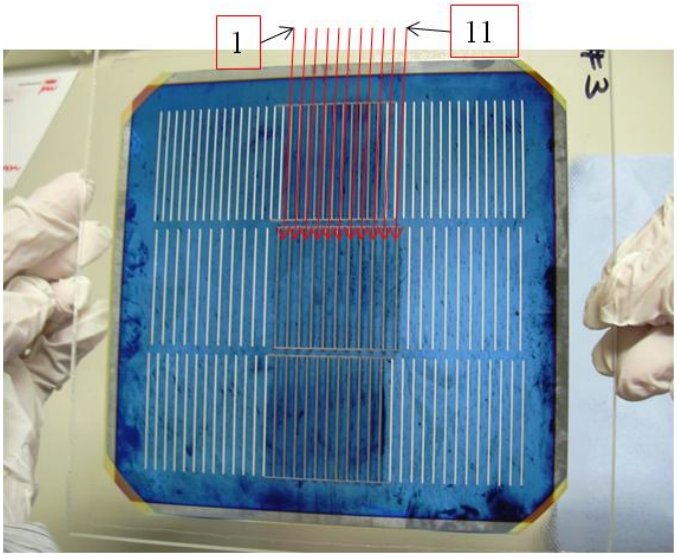

Fig. 5. Rear side of first realized XIS demonstrator mini-modules. Three mini-modules are realized in one wafer, with 3 mm strip width (top), 4 mm strip width (middle) and 3.5 mm strip width (bottom). Each mini-module consists of 10 strips / cells and 11 metal fingers (as indicated) forming the interconnection and measurement positions.

The results were analyzed further by monitoring of the minority carrier lifetimes of the devices. Two main issues were identified. One issue is that upon deposition of SiNx on the front side and in the grooves, also parasitic deposition on the rear occurs. This results in poor properties for the heterojunction emitter. Another issue that was encountered is lifetime degradation induced by the rear side laser processes.

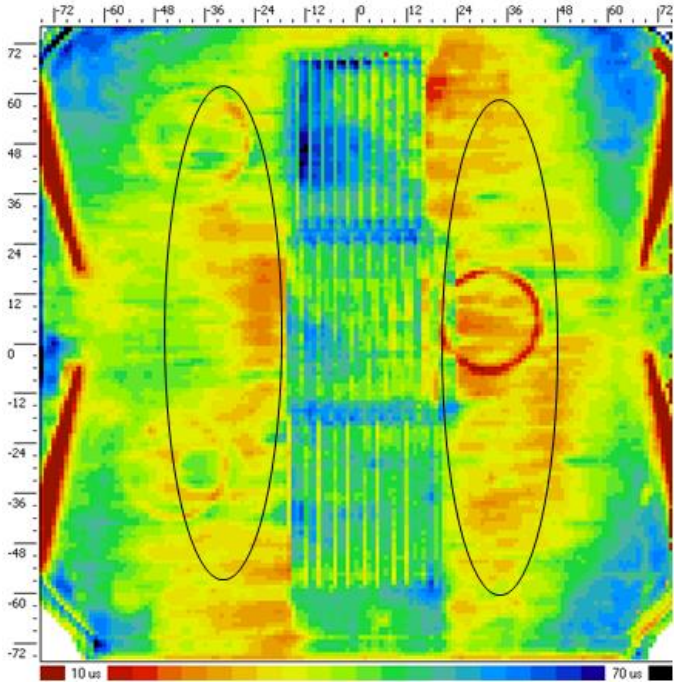

Fig. 6a. Lifetime mapping of three XIS minimodules from top to bottom in the middle of the wafer before the last process steps.

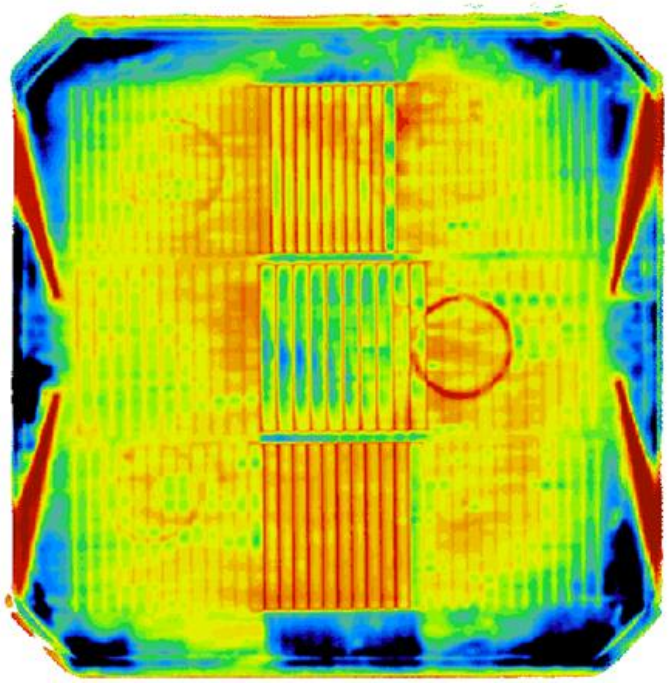

Fig. 6b. Lifetime mapping of three XIS minimodules from top to bottom in the middle of the wafer after the last process steps, same scale as in Fig. 4a.

In Fig. 6 lifetime mappings of the mini-modules and the surrounding wafer are shown before (a) and after (b) the rear last process steps. After these steps, the lifetimes of the strips in the mini-modules was reduced. The effect of parasitic nitride deposition can best be seen in the areas of the wafer next to the mini-modules, indicated by the black lines, and in the 'cloud' area in Fig. 7. The degradation of the lifetime as seen in Fig. 6 seems the least severe for the broadest (4 mm) strips. This was investigated in some more detail. In Fig. 7 line scans of the lifetimes are shown in the direction perpendicular to the strips, before and after the last rear process steps. The difference in lifetime is largest for the smallest strips. We assume that this effect is due to the confinement of heat in the strips, inducing damage to the amorphous emitters after lamination of the devices to the glass plate with EVA. In other experiments we have observed that the amorphous silicon layers that we have been employing are sensitive to anneal at temperatures lower than 200 °C. In Fig. 6a and Fig. 6b also ring-shaped markings can be seen, indicating some imperfections in the diffusion process. However, this is known to have only a minor effect on the performance. We attribute the overall low performance mainly to the emitter quality, as a result of the rear surface being exposed to nitride before amorphous silicon deposition and to amorphous silicon layers that are relatively sensitive to the impact of the heat that is applied after deposition. Our further efforts are directed to

process flows that allow clean surfaces before amorphous silicon deposition, and to amorphous silicon layers that are more tolerant to heat impact and with higher performance.

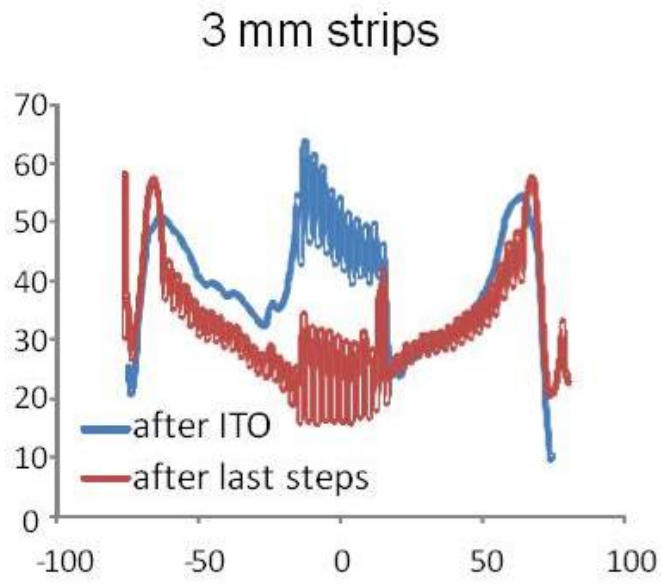

Fig. 7a. Lifetime scans in the direction perpendicular to the strips before (blue) and after (red) the last process steps, for 3 mm strips.

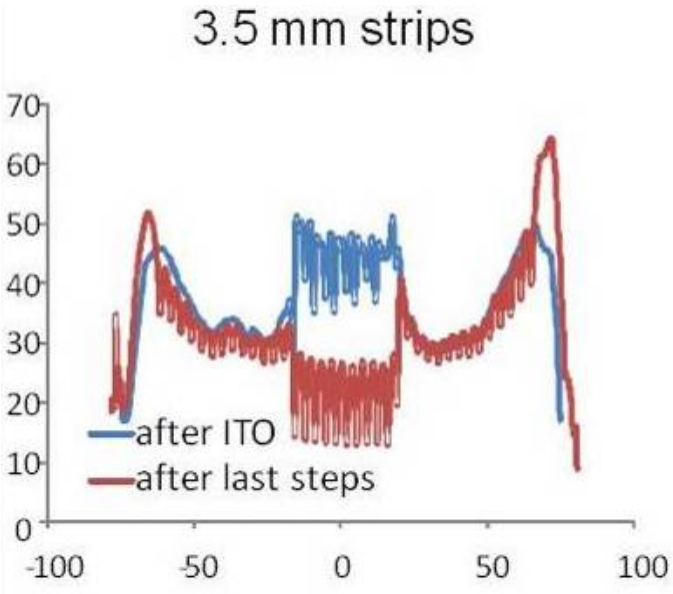

Fig. 7b. Lifetime scans in the direction perpendicular to the strips before (blue) and after (red) the last process steps, for 3 mm strips.

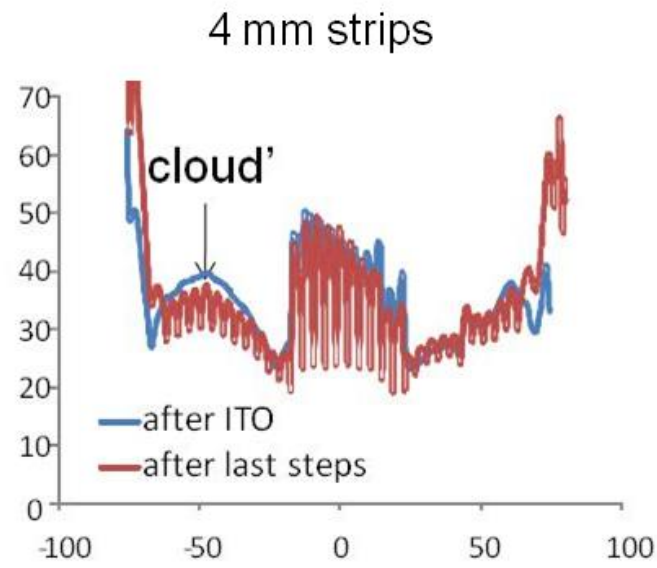

Fig. 7c. Lifetime scans in the direction perpendicular to the strips before (blue) and after (red) the last process steps, for 4 mm strips.

VII. Conclusion and Outlook

The XIS concept has been introduced. It has the potential to achieve a significant cost reduction with high efficiency back-contact heterojunction silicon thin wafer technology, cutting down the bill of materials, almost eliminating the use of expensive metals, and thin film like, large area high throughput production technology. First laboratory devices have been made, demonstrating series connection of over ten individual hybrid back contact silicon heterojunction solar cells, indicating that all features have proven to be functional, including realization of a hybrid BC-HJ structure, groove formation, groove passivation, and series connection.

The long term potential of XIS is an integrated cell and module concept that combines the high efficiency of thin crystalline silicon wafers with low costs and large scale potential. For the short term, standard wafer thicknesses can be used. Full size module processing is not necessary but for the last step. Therefore, standard wafer processing equipment can be used to realize high efficiency back contact heterojunction cells. The major advantage compared to standard technology is the complete or almost complete elimination of silver and other metals.

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