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# INDUSTRIALLY FEASIBLE >19% EFFICIENCY IBC CELLS FOR PILOT LINE PROCESSING

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## ABSTRACT

Interdigitated Back Contact (IBC) solar cells with >19% efficiencies have been fabricated using n-type silicon wafers and well-demonstrated high-volume solar cell process technologies alone. Excellent current collection is implied by $J_{sc}$ values as high as 41.6 mA/cm$^2$. High Pseudo Fill Factors (PFF) of above 81% and reduced Fill Factors (FF) of below 72%, suggest that the primary losses are due to series resistance. The process flow described is currently being transferred to a pilot production line for further process development.

## INTRODUCTION

Silicon solar cell cost-per-watt is still significantly higher than coal-produced power, which is the baseline cost of today's commercial electricity. To be a competitive energy source, solar cell conversion efficiencies must increase while maintaining a reduced cost, mainly via improving cell design and minimizing silicon content. In order for this to be undertaken, new fabrication strategies, processing steps and materials need to be introduced to the high-volume manufacturing arena.

Since 2009, Siliken and ECN have been working in collaboration to develop an industrially feasible process flow for IBC cells on n-type Cz monocrystalline silicon wafers. In parallel, Siliken has been building a pilot production line to explore both mainstream and alternative cost-effective processing approaches that can be scaled to production while reaching stabilized efficiencies beyond the 20% benchmark. Indeed, IBC cell designs using n-type wafers have been demonstrated to enable production efficiencies as high as 24.2% [1-4], although to date only Sunpower Corp. worldwide have successfully implemented their proprietary fabrication approach in manufacturing [1]. Among other high-efficiency silicon solar cells concepts, the IBC design offers the highest efficiencies demonstrated to date in production, mainly by eliminating front shading losses by placing all contacts at the back of the device. However IBC cell fabrication entails key challenges which include high resolution patterning and alignment of regions for both n- and p-type diffusions and contacts, as well as excellent passivation for different types of diffusions on the same surface.

In this work we show that efficiencies of >19% can be achieved by fabricating IBC cells using currently well-established manufacturing process technologies alone, such as wet-processing, tube furnace diffusions, plasma enhanced chemical vapor deposition (PECVD) and screen printing for both metallization and patterning. Best cell results are presented and the primary loss factors analyzed using both characterization techniques and simulations. The results show that >20% efficiencies are possible if the series resistance is decreased. Furthermore, alternative patterning and deposition process technologies, featured at the pilot line, will be described and discussed as possible enablers for beyond 20% efficiencies IBC cell technology.

## EXPERIMENTAL

IBC cells were fabricated at ECN laboratories using n-type wafers supplied by SUMCO with a thickness of 180 µm and resistivity ~ 2 Ω-cm.

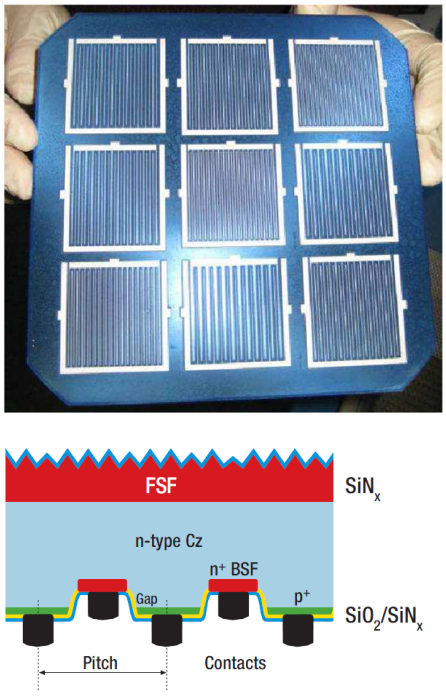



**Figure 1. (At top) Image of a 156 x 156 mm$^2$ wafer with a matrix array of 3 x 3 IBC cells. The lower image shows a schematic of the IBC cell architecture, indicating the Front Surface Field (FSF), n$^+$-Back Surface Field (BSF), p$^+$ -emitter, contacts and passivating layers. The definition of pitch and gap are also included.**

Figure 1 shows an image of a 156 mm semisquare wafer with a 3 x 3 array of IBC cells (each with an area of 13.24 $cm^2$). By using this matrix design 9 different configurations of IBC cells were fabricated on each wafer, allowing for >1000 cells to be evaluated.

The process flow (Fig. 2) included initial cleaning and texturing, followed by Front Surface Field (FSF) diffusion, masking, diffusion and patterning of the emitter and BSF, passivation of both the front and back surfaces of the cell, and finally metallization with screen printing and firing. Optimization experiments were focused particularly on (1) the pitch and emitter fraction, (2) the cell passivation, and (3) the front surface field (FSF). Characterization was carried out using standard techniques such as Photoluminescence/ Electroluminescence (PL/EL), Light Beam Induced Current (LBIC), Quasi-Steady-State Photoconductance (QSSPC) and spectral response, as well as by means of 2D simulations to support the experimental work. The cell design varied in terms of emitter fraction (67-80%), pitch (2-3 mm), gap (150-300µm) and passivation type. In the present contribution passivation schemes using $SiO_2$+$SiN_x$:H [5] will be presented, while other passivation alternatives and further analysis will be presented elsewhere [6]. In this article we present best cell results highlighting the primary loss mechanisms and describe further processing techniques to improve cell efficiency that are currently being develop in a pilot production line.

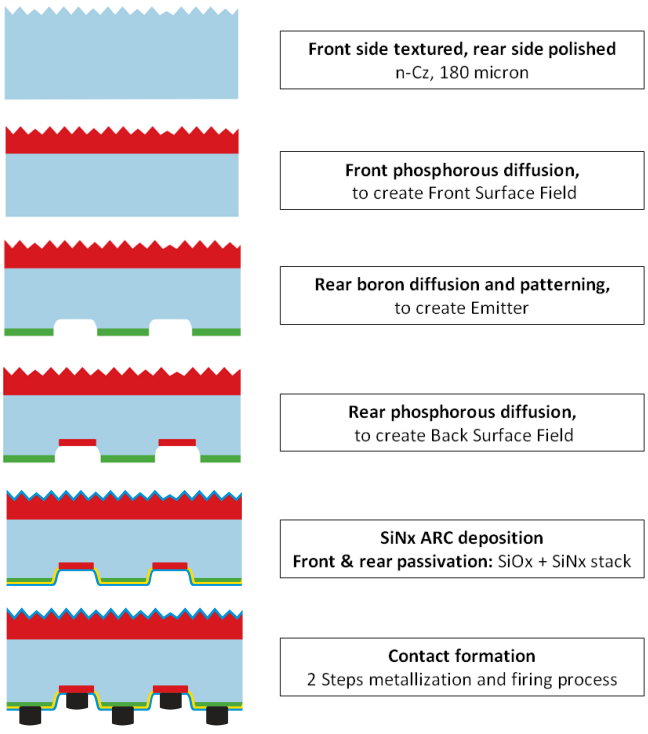
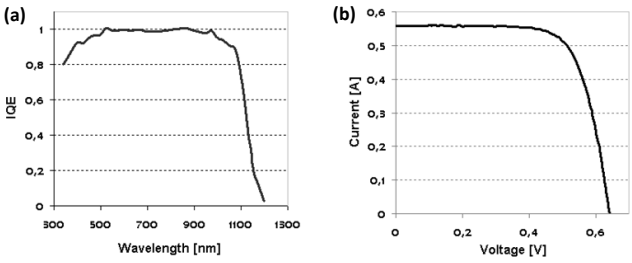



**Figure 2. Process flow used for fabricating >19% interdigitated back contact solar cells.**

## RESULTS

To achieve an ideal FSF, the initial surface phosphor doping concentration was tailored according to a diffusion profile derived from 2D simulations. Figure 3 shows both (a) Internal Quantum Efficiency (IQE) and (b) IV data, as well as a summary of measured parameters corresponding to a best cell of 19.1% efficiency. For this cell the emitter fraction was 80%, the pitch was 2 mm and a $SiO_2$+$SiN_x$:H stack was used to passivate the emitter, base and BSF. The IQE results are very good reaching unity, with a characteristic drop in the red close to the band gap limit. Superb current collection is shown by a $J_{sc}$ value as high as 41.6 mA/$cm^2$, measured using an in-house technique, and spectral mismatch measurements later confirmed a mismatch correction of only 0.3%, verifying a $J_{sc}$ of 41.5 mA/$cm^2$.The $V_{oc}$ of 641 mV may be limited due to the fire through contacts, or non-optimal passivation of the emitter, BSF and gap. Alternative advanced passivation schemes may further improve the $V_{oc}$, since the emitter fraction is large, and the positive charges in the nitride are more suitable to passivating n-type layers. The results show high Pseudo Fill Factors (PFF) of above 81% but lower Fill Factors (FF) of below 72%, which indicates that the primary losses are due to series resistance.




| Pitch [mm] | Area ($cm^2$) | Isc (A) | Jsc (mA/$cm^2$) | Voc (V) | Jsc * Voc (mA* V/$cm^2$) | FF | Eta (%) |
|---|---|---|---|---|---|---|---|
| 2 | 13,2 | 0,551 | 41,6 | 0,641 | 26,7 | 0,715 | 19,1 |

**Figure 3. a) IQE, b) IV and table of measured parameters corresponding to the best IBC cell fabricated.**

Overall experimental results show that several factors play an important role in obtaining high efficiency including high emitter fraction, low pitch and high bulk lifetime. Moreover, typical values of the FF for similar IBC cells are closer to 0,8 [3, 4], which suggest that further efficiency improvements are feasible.

As shown in figure 4, series resistance is present in many forms within the cell, including in the emitter and BSF contact resistance, the emitter and BSF internal resistance, the base resistance through the thickness and parallel to the plane, as well as the series resistance through the FSF. In order to reduce the series resistance further work needs to be carried out to investigate the relative contributions shown schematically in Figure 4 and minimize the mayor contributions.

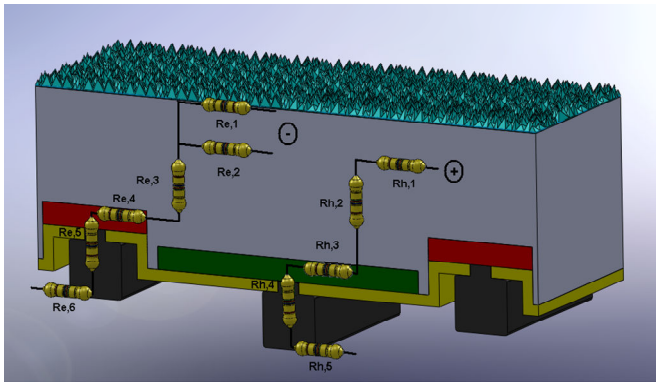



**Figure 4. Schematic 3D architecture of the device with a superimposed circuit model showing resistor corresponding to each contribution to the series resistance along the electron and hole paths, respectively. The resistors in the electrons path represent: Re6 (n-metal finger), Re5 (n-contact) , Re4 (Lateral BSF) , Re3 (vertical base), Re2 (lateral base), and Re1 (lateral FSF); and in the case of the hole path: Rh5 (p-metal finger), Rh4 (p-contact), Rh3 (lateral emitter), Rh2 (vertical base), and Rh1 (lateral base).**

Modeling of the cells was undertaken using the 2D simulation software MicroTec [7]. Figure 5 shows (a) the Fill Factor (FF), (b) open circuit voltage, (c) the current density and (d) efficiency versus the pitch for both 2 and 10 Ω.cm base resistivity. The model includes a front surface field (FSF) of 150 Ω/sq, a cell thickness of 185 µm, and diffusion profiles transferred directly from the measured SIMS profile. Different surface recombination velocities were input according to the different diffused regions. The BSF and the gap (the distance between emitter and the BSF) were kept constant at 250 µm and 150 µm respectively, and the pitch and emitter fraction varied. It should be noted that in these simulations the emitter fraction and pitch are by definition interlinked, with a larger pitch implying larger emitter fraction. The model evaluates only the semiconductor part of the cell, with the metal contacts excluded.

Figure 5(a) shows that the fill factor decreases as the pitch increases, since the emitter fraction is larger and the majority carriers have to travel a longer path to reach the BSF. Figure 5 (b) and (c) indicate that the collected current and open circuit voltage increase as the pitch is increased, and the current shows a larger dependency on the base resistivity. Since the efficiency includes contributions from the FF, current density and voltage, Figure 5 (d) shows a maximum efficiency at a pitch of ~ 1500 µm. This efficiency peak represents equilibrium between increased series resistance losses for larger pitches and reduced $V_{oc}$ &current density for smaller pitches. An efficiency enhancement can be observed when the bulk resistivity is increased, which indicates that reduced recombination into the bulk can overcome the detrimental effect of the increased series resistance losses.

The results clearly indicate that the resolution of the BSF and gap play an important role since they limit the possibility of reducing the pitch further. Further investigation in order to minimize the size of the BSF and gap is recommended, as well as simulations to explore the effect of pitch and emitter fraction independently.

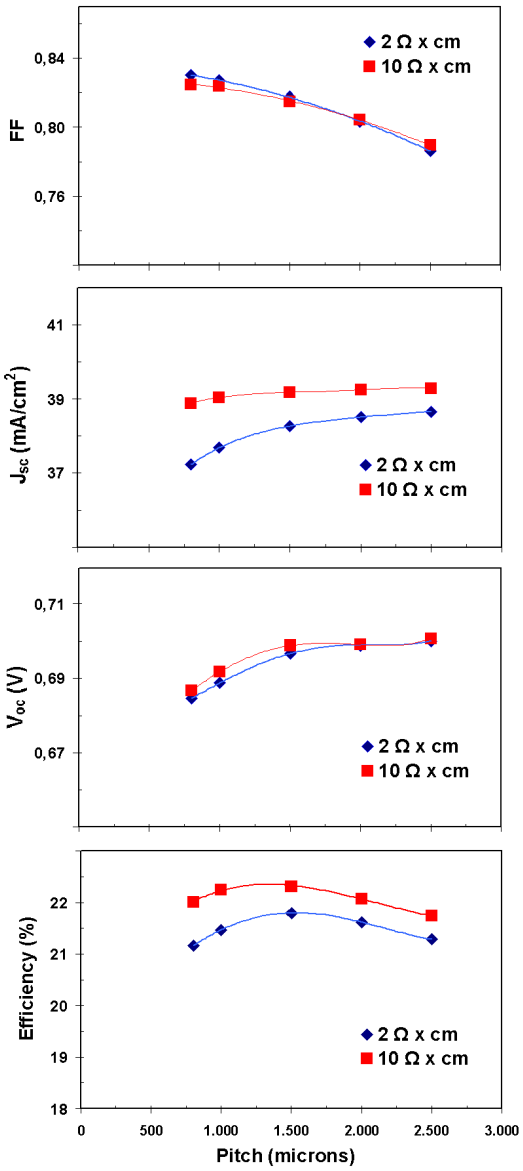



**Figure 5. 2D simulations results showing the variation versus pitch of (a) Fill factor (FF), (b) Short circuit current ($J_{SC}$), (c) Open circuit voltage ($V_{oc}$) and (d) efficiency for base resistivities of 2 Ω x cm and 10 Ω x cm, respectively.**

Although IBC cells avoid optical shading losses by placing the metal grids on the backside of the cell, electrical shading losses still exist [8]. This is due to rear side recombination in the regions of the base fingers. Figure 6 presents the light

beam induced current (LBIC) maps on the back of one of the cells. The highest IQE is seen in the region of the emitter (blue), the lowest in the BSF (red), with intermediate values in the gap (green). Both the experimental and simulation results indicate that reducing the size of the BSF and gap will help to increase the efficiency of the cell, although this can be a challenge for screen printing since the resolution is limited.

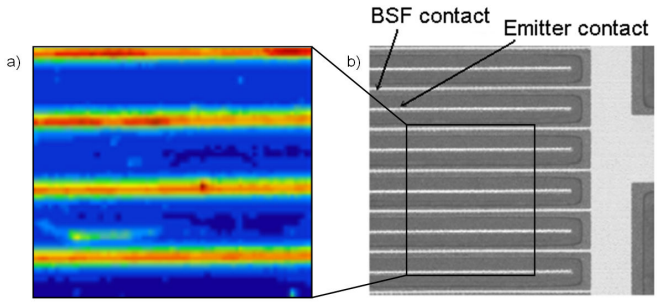



**Figure 6. (a) LBIC measurement and (b) optical image showing difference between losses on BSF and Emitter contacts.**

Currently, the process described is being transferred to Siliken's high-efficiency pilot production line. The facility consists of an ISO-7 clean room and custom-designed batch tools with minimum throughputs exceeding 200 wafers/hour. The facility is designed to evaluate cost effective production routes for >20% efficiency IBC cells, as well as other high efficiency concepts such as Laser-doped Selective Emitter (LDSE), Passivated emitter Rear Contact (PERC) and Heterojunction Intrinsic-Layer (HIT) concepts. In addition to the process technologies used for the fabrication of the IBC cells described in this manuscript, the pilot line features alternatives thin film deposition and patterning approaches, such as sputter deposition (PVD) and reactive-gas etching (dry-etching), respectively. Both the PVD and dry-etching tools have been designed and built by Siliken as Original Equipment Manufacturer (OEMs) and are based in ultra-high-vacuum chambers with base pressures <5 x $10^{-8}$Torr. Sputtering technology is a well proven deposition technology in PV manufacturing and has been demonstrated for both passivation and even high-throughput metallization [9]. The custom PVD tool allows for multiple-material stacks based on both metals and oxides, as well as advanced in-situ thermal processing. This tool will be used to explore both advanced passivation and metallization schemes for IBC solar cells. On the other hand, dry-etching also has a history in PV manufacturing particularly for batch edge-isolation. The custom-designed tool at the line uses inductively-coupled plasma technology for enhanced etch rates and homogeneity and it will be used for both advanced texturing and pattern transfer applied to IBC cell processing.

## CONCLUSIONS

The results show that 19.1% efficiency IBC cells have been successfully fabricated using low cost fabrications techniques such as screen printing for patterning to create the p-n fingers and metallization. In general the results show higher efficiencies for larger emitter fraction and smaller pitch, with optimum results in this study obtained for an emitter fraction of 80%, and a pitch of 2 mm. The cell was passivated with $SiO_2$+$SiN_x$:H for the emitter, BSF and gap, and excellent Jsc values of 41.5 mA/cm$^2$ have been achieved. The IQE results show close to unity, which is to be expected for an IBC cell with all the contacts positioned on the back-side. The high PFF and low FF indicate that the primarily losses are due to series resistance, and if the fill factor can be increased to 80% efficiencies of >21% can be achieved.

Simulations show that the fill factor can be increased by decreasing the pitch, and the optimum was obtained when the pitch became comparable to the size of the BSF. Increasing the resolution of the BSF and gap may further enhance the fill factor. LBIC results indicate that electrical shading occurs in the region of the BSF and gap, and that high resolution patterning to decrease the size of the BSF and gap would increase the IQE.

In summary the results indicate that three factors may significantly increase the efficiency of the IBC cells: (1) decreasing series resistance, (2) increasing the resolution of the BSF and gap, and (3) investigating advanced passivation schemes.

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