BEHIND (BACK ENHANCED HETEROSTRUCTURE WITH INTERDIGITATED CONTACT) SOLAR CELL

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ABSTRACT: In this paper we investigate in detail how the heterostructure concept can be implemented in an interdigitated back contact solar cell, in which both the emitters are formed on the back side of the c-Si wafer by amorphous/crystalline silicon heterostructure, and at the same time the grid-less front surface is passivated by a double layer of amorphous silicon and silicon nitride, which also provides an anti-reflection coating. The entire process, held at temperature below 300 °C, is photolithography-free, using a metallic self-aligned mask to create the interdigitated pattern. An open-circuit voltage of 695 mV has been measured on this device fabricated. The mask-assisted deposition process does not influence the uniformity of the deposited amorphous silicon layers. Several technological aspects that limit the fill factor are considered and discussed.
Keywords: heterostructure, IBC, amorphous silicon.

1. INTRODUCTION

The tendency towards shrinking wafer thickness to reduce the photovoltaic cost, is driving solar cell fabrication to reduce the process temperature. This in particularly for multi-crystalline silicon where wafer bowing and thermal stresses in the bulk material can be problematic. On the other hand, an effective back surface field, usually provided by high temperature processes, is an increasing necessity with decreasing substrate thickness. Both of these issues can be faced with amorphous/crystalline (a-Si/c-Si) silicon heterostructure, which can be deposited by Plasma Enhanced Chemical Vapour Deposition (PECVD) at temperature below 400 °C. A way to increase PV conversion efficiency is represented by rear-junction, back-contact solar cell design interdigitated (IBC) able to collect photogenerated carriers entirely from the rear of the cell. The advantages of this structure include no contact grid shading on the sunward side and use of a thin substrate, [1, 2]. Another useful concept for increasing c-Si based solar cells is the one adopted by Sanyo's HIT structure in which high-quality intrinsic a-Si:H layers allow an excellent surface passivation of c-Si surface, resulting in high efficiency, especially a high open circuit voltage (V_{oc}): almost 730 mV has been reached [3]. This technology has been demonstrated effective both on n-type or p-type crystalline silicon [4, 5]. Moreover the temperature coefficient of a-Si:H / c-Si heterostructure cells is better than conventional c-Si solar cells and results in a higher output power at high temperatures [6]. Finally the implementation of a-Si:H / c-Si heterojunction as solar cell concept has the capability of reaching efficiencies up to 25% [7]. Even if such technology can increase the open-circuit voltage, the a-Si window layer can still affect the short-circuit current due to the amorphous silicon absorption in the blue region of the solar spectrum. To overcome this and to remove any shadowing effect from a top metal grid, we have developed a new cell design transferring the emitter and both contacts to the rear side of the device: the BEHIND (Back Enhanced Heterostructure with InterDigitated contact) solar cell. Our approach to BEHIND cell fabrication is based on the idea to develop an innovative IBC technology entirely performed at very low temperature (< 300 °C), thus resulting in an advantage for thinner wafers; involving a self-aligned mask assisted and photolithography-free process and that could benefit of the passivation quality of the a-Si:H. If the rear-junction and backside contact design enjoys reduced optical shading losses, also requires high bulk lifetime and low front-surface recombination. In particular this work has been devoted to overcome several problems that strongly affected the previously reported structure [8], such as p-type c-Si p-type a-Si base contact, shunt effect and series resistance, in order to achieve a reliable solar cell process.

2. DEVICE FABRICATION

Actual BEHIND solar cell has been fabricated starting from a 4 inch diameter, 200 µm thick, <100> oriented, 1 Ωcm p-type, one side polished CZ mono-crystalline silicon wafer. After front side alkaline texturing and industrial cleaning, the front side antireflection passivation coating and the rear side emitter and back contact have been deposited in a 13.56 MHz direct Plasma Enhanced Chemical Vapour Deposition (PECVD) system. In particular a double layer stack of a-Si/SiN_x on the sunward side, acting as passivation and anti-reflection layer [9] has been deposited using the conditions reported in table I. Then on the whole polished backside of the wafer, after an HF-dipping procedure to remove the native oxide, an intrinsic a-Si:H buffer layer has been deposited followed by a n-type doped a-Si:H one. Over this film a chromium silicide (CrSi) layer has been formed to increase the emitter conductivity [10] by Cr evaporation and wet removal. At this stage a metallic mask has been held and fixed by a particular holder on the rear side of the device. This mask, fabricated from a 100 µm thick Molybdenum foil, has a comb shaped aperture obtained by Nd-YAG laser ablation. A dry etching procedure using NF_3 gas has been performed to remove the n-type a-Si:H portion not covered by the mask, using settings defined on the base of previous experiences [11]. Subsequently, keeping the mask in the same position, the cell base contact has been formed by

Table I. PECVD deposition parameters used in the thin film formation (temperature indicated are effective).

Layer		Gas	Flow (sccm)	Pressure (mTorr)	Temperature (°C)	RF Power (mW/cm^2)	Thickness (nm)
Front side	a-Si:H	SiH_4/Ar 5%	120	750	250	36	10
	SiNx	SiH_4/Ar 5%,NH_3	120, 10	750	250	36	65
Rear side	a-Si:H	SiH_4/Ar 5%	120	750	250	36	5
	n-a-Si:H	SiH_4, PH_3	40, 10	300	200	28	20
	a-Si:H	SiH_4/Ar 5%	120	750	250	36	5
	p-a-Si:H	SiH_4, B_2H_6	40, 4	680	170	28	10
	δn a-Si:H	SiH_4, PH_3	40, 10	300	200	28	5

an intrinsic a-Si:H buffer and a p-type a-Si:H layers, followed by a δn-a-Si:H deposition useful to increase the amorphous conductivity [10]. All the deposition conditions of the above mentioned layer in Table I are summarised. Then another comb shaped aperture mask, having narrower fingers with respect to the previous mask, has been held and fixed on the rear side of the device using the previously used holder. The aperture of each finger of this second mask is about the half of the first mask leading to not difficult mechanical alignment with the pattern underneath.

Through these aperture a 30 nm thick Cr followed by 4 μm Al layers have been evaporated. The Cr is used to form the CrSi layer on the p-type a-Si:H layer [10]. Finally, the mask has been rotated 180 degrees and 4 μm of Ag has been evaporated to contact the emitter region, creating the interdigitated shape with respect to the base contact. The total area of the solar cell is 6.25 cm^2. A schematic cross section of the BEHIND cell in Figure 1 is depicted. At this stage the BEHIND cells have been characterized in terms of current-voltage (I-V), both in dark and AM1.5G conditions, reflectance and Quantum Efficiency (IQE: Internal Quantum Efficiency; EQE: External Quantum Efficiency).

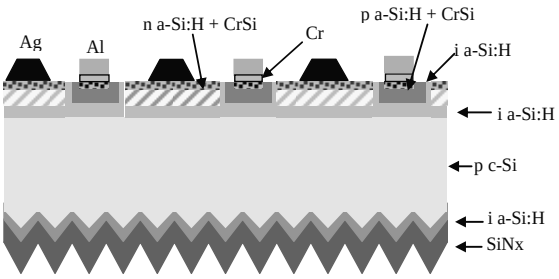

Figure 1. Schematic cross section of the BEHIND cell.

3. RESULTS AND DISCUSSION

The experimental I-V characteristic has been measured at room temperature, under Class A calibrated to 1000 mW/cm^2 and AM1.5g illumination and in Figure 2 is shown as symbols. Taking into account the best result of a silicon based interdigitated solar cell [1] we can see that the very high open circuit voltage Voc = 695 mV confirms the effectiveness of the a-Si/c-Si heterojunction as the way to improve the silicon based solar cell efficiency. This result also confirms that the uniformity of the deposited amorphous silicon layers is not influenced by the mask-assisted deposition process even when multiple masks are used in the fabrication process. Indeed the alignment between masks and substrate is feasible and the regions where the doped layers can unfortunately overlap are isolated by the intrinsic a-Si:H. The introduction of CrSi on p-type a-Si:H base contact has allowed to overcome the necessity of laser treatment to obtain an effective base contact [8]. This effect is more evident considering the band bending distribution at the p-S-Si/i-a:Si:H/p-a-Si:H interface, as simulated with a finite difference software [5] and reported in Figure 3 before (a) and after (b) the CrSi introduction at 1 sun illumination conditions. The CrSi layer enhances the tunnelling mechanism at the interface, resulting in a better hole collection.

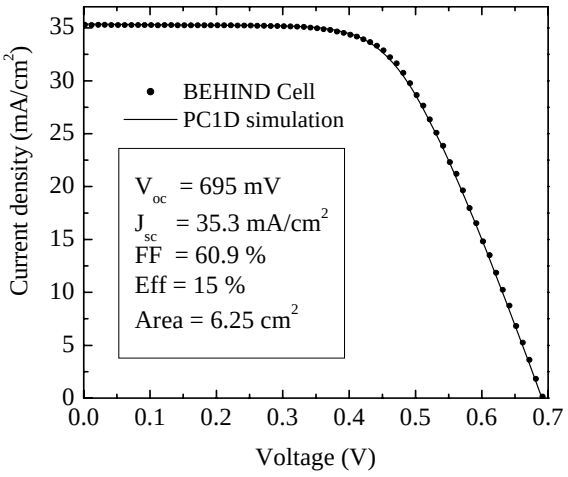

Figure 2. I-V measurements and photovoltaic parameters under AM1.5G condition: experimental data (symbols) and PC1D simulations (lines).

Moreover the CrSi formation on n-a-Si:H layer has produced an equipotential emitter surface that reflects in a higher cell Fill Factor (FF) by lowering the series resistance. As expected the short circuit current J_{sc} is higher than that collected by a grid shaped front contact cell, but in principle should be higher, so optical and recombination losses still affect the cell. To get better inside the limiting factor for J_{sc} a detailed analysis of the EQE has been performed using PC1D software [12]. The key issues to obtain high J_{sc} depends on diffusion length, L_d, and surface recombination velocity, $S_{n,p}$. To explore the effect of both parameters we have compared the EQE experimental data with a PC1D simulation, in which we have simplified our BEHIND cell into one dimensional crystalline based solar cell having a back thin n-type aSi:H emitter layer.

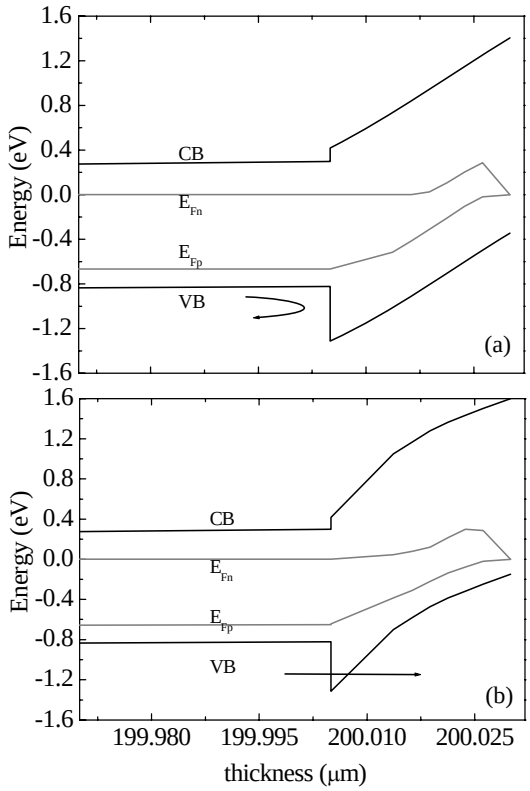

Figure 3. Band bending distribution before (a) and after (b) CrSi introduction simulated at 1 sun illumination condition.

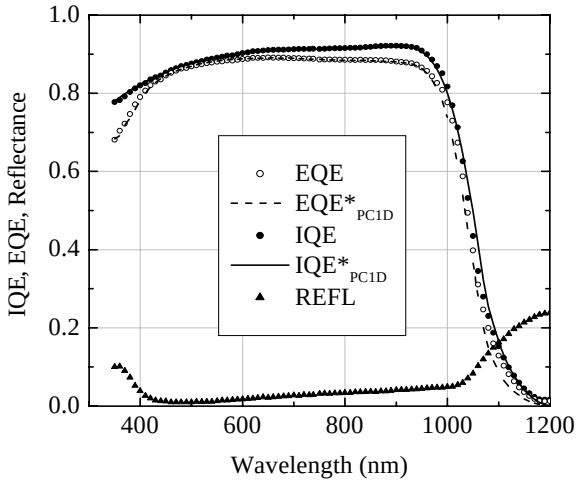

Figure 4. IQE, EQE, Reflectance of the BEHIND cell: experimental data (symbols) and PC1D simulations (lines).

A detailed description of parameters adopted in the simulation is reported in Table II. Those parameters have been fixed on the based of both c-Si and a-Si:H properties and on geometrical characteristic of the cell. The majority of parameters reported in Table I are commonly used in literature for both c-Si and a-Si:H materials [5]. Choosing appropriate L_d and $S_{n,p}$ values, and taking into account the measured reflectance profile, reported in Figure 4 as symbols, we have obtained a good agreement between experimental data and simulation model, except in the region of higher energy photons, since the simulation does not account for the passivation/antireflection coating absorption. So at the end of simulations, EQE, IQE data have been reduced by the a-Si:H thin layer (d = 3 nm) absorption and reported as EQE*and IQE* in Figure 4.

Table II Parameters used in PC1D simulation.

c-Si parameters	
thickness (μm)	200
mobility μ_n , μ_p (cm^2/Vs)	1417, 470
bandgap (eV)	1.124
intrinsic conc. n_i (cm^{-3})	$1 \cdot 10^{10}$
p-type doping (cm^{-3})	$3.2 \cdot 10^{16}$
diffusion length L_d (μm)	680
front surf. rec. S_n,S_p (cm/s)	80
rear surf. rec. S_n,S_p (cm/s)	$1 \cdot 10^{6}$
a-Si:H parameters	
thickness (μm)	0.015
mobility μ_n , μ_p (cm^2/Vs)	1, 0.1
bandgap (eV)	1.65
intrinsic concentration ni (cm^{-3})	$1 \cdot 10^{7}$
μτ (cm^2/V)	$1 \cdot 10^{-12}$
n-type doping (cm^{-3})	$5 \cdot 10^{17}$
n^+-type doped (CrSi)	$5 \cdot 10^{18}$

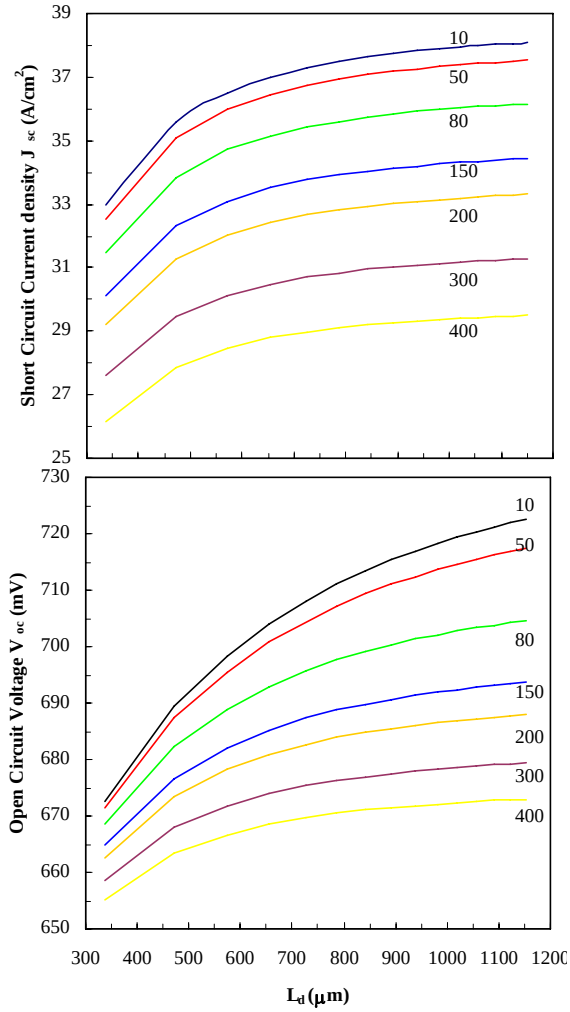

Figure 5. PC1D simulations of J_{sc} and V_{oc} values as a function of L_d for different values of front side $S_{n,p}$ (cm/s) reported close to each curve.

In this improved version of the cell with respect to the previously shown in ref [8] the EQE curves does not show any hump related to the depletion region at the edge of the emitter in the spectral region ranging from 900 nm to 1000 nm as commonly appears on rear emitter cell having not sufficiently high L_d and not optimized finger number per square centimetres in the interdigitated rear geometry. This confirms the goodness of the actual fabrication process. Moreover the Reflectance profile measured and reported in Figure 4 remarks the efficacy of the texturization and antireflection coating, leading to an effective value of 4.6% if compared with the sunlight spectrum. The PC1D model is now able to predict the J_{sc} and V_{oc} by varying the L_d and front side $S_{n,p}$ as depicted in figure 5. The model suggests that the front side $S_{n,p}$ affects the device performances more with respect to L_d. Indeed while a L_d value of 500 μm is acceptable to collect the photogenerated carriers over the entire spectrum from 350 nm to 1200 nm, $S_{n,p}$ values higher than 100 cm/s strongly decreases the J_{sc} values reducing the advantage of front metal grid absence. To obtain high efficiency solar cell the model suggests that $S_{n,p}$ down to 10 cm/s and L_d around 1 mm are needed to achieve J_{sc} and V_{oc} values of 38 mA/cm^2 and 720 mV respectively.

The second mask used for the metal deposition over the p-type a.Si:H base contact has been very helpful to reduce the shunt effect at the edge of the p and n contact that now are more pronounced due to increased n-type a-Si:H layer conductivity. Although this shunt effect is still evident from the I-V measurement performed in dark condition reported in Figure 6. In fact the dark current mainly flows between the fingers shaped back contacts. For this reason the area used in I-V dark evaluation is only that of the p-type base contact.

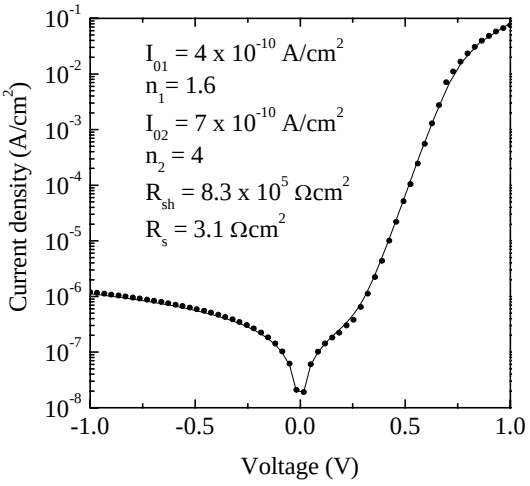

Figure 6. Experimental (symbols) and modelled (line) I-V characteristic at room temperature and dark conditions.

The I-V measurement can be modelled by the two diode model plus a series and a shunt resistance contributes.

$$I(V) = I_{01}\left(e^{\frac{V}{n_1 V_T}} - 1\right) + I_{02}\left(e^{\frac{V}{n_2 V_T}} - 1\right) + \frac{V}{R_{sh}}$$

Where I_{01} is the diode reverse saturation current; I_{02} accounts for recombination thermal generation currents in the depletion region; R_{sh} is the shunt resistance, n_1, n_2 are the ideality factors and V_T is the thermal equivalent voltage. By iterative solution it is possible to evaluate also the series resistance R_s. The parameter values used to fit the experimental data in the inset of Figure 6 are listed. At high current injection level the transport mechanism is dominated by the series resistance, as already seen in the lighted IV curve.

4. CONCLUSIONS

In this paper we have shown the actual improvement of the BEHIND cell concept in which a-Si:H/c-Si heterostructures have been used to form an interdigitated emitter and base contacts. The grid-less front surface now ensures as high I_{sc} value as 35.3 mA/cm^2 due to improved diffusion length. With the aid of a PC1D model we have deduced that front surface recombination still limits the J_{sc} and we have also evaluated the effectiveness of CrSi to increase the transport reducing the series resistance. In turn, to form this layer, a secondary mask has been needed but this does not reduce the effectiveness of mask-assisted deposition process. Actually a V_{oc} of 695 mV has been reached, that can be considered a further improvement respect to the previous results to continue to develop this low temperature process helpful to reduce the PV manufacturing cost.

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