1 € PER WATT-PEAK ADVANCED CRYSTALLINE SILICON MODULES: THE CRYSTALCLEAR INTEGRATED PROJECT

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ABSTRACT: CrystalClear is an Integrated Project carried out in the 6th Framework Program of the European Union. The main project aim is to reduce the direct manufacturing costs of crystalline silicon PV modules to 1 €/Wp, when produced in next-generation plants. CrystalClear deals with the entire crystalline silicon value chain from silicon feedstock up to module manufacturing. In the course of the project, which started in 2004, several 'overall' technologies have been defined and developed. These technologies represent different combinations of wafer options, cell and module designs as well as processing approaches. They have been analysed in terms of their manufacturing costs, assuming large-scale production. It is found that crystalline silicon PV technology has the potential to reach direct module manufacturing costs of around 1 €/Wp on a relatively short term (i.e. within ≈5 years). This implies that wafer-based crystalline silicon photovoltaics is compatible with the requirements to achieve grid parity, see the Strategic Research Agenda of the PV Technology Platform, www.eupvplatform.org. Critical conditions to reach this cost level are: efficient silicon utilization (g/Wp module power), high total area module efficiency and high-throughput, high-yield production.

Keywords: Cost Reduction, PV Module, Silicon Solar Cell, EU Project.

1 THE CRYSTALCLEAR PROJECT

CrystalClear is a large, 5-year joint effort of a powerful consortium of European companies, research institutes and university groups involved in crystalline silicon PV technology, see [1] and www.ipcrystalclear.info. It is an Integrated Project carried out in the 6th Framework Program of the EU. The overall aims of CrystalClear are:

- research, development, and integration of innovative manufacturing technologies that allow solar modules to be produced at a cost of 1 €/Wp in next generation plants;
- improvement of the environmental profile of solar modules by the reduction of materials consumption, replacement of materials and designing for recycling;
- enhancement of the applicability of modules and strengthening of the competitive position of photovoltaics by tailoring to customer needs and improving product lifetime and reliability.

Realisation of these aims is a necessary condition for the European PV industry to maintain and strengthen its position on the world market and for photovoltaics to fulfil the expectations and policy targets.

CrystalClear runs from January 2004 to June 2009 and has a total budget of 28 M€. Of this amount 16 M€ will be contributed by the EU and 12 M€ by the 16 partners:

Industry partners:
- BP Solar (ES);
- Deutsche Cell (DE);
- Deutsche Solar (DE);
- Isofotón (ES);
- Photowatt (FR);
- REC (NO);
- ScanWafer (NO);
- Schott Solar (DE);
- SolarWorld Industries (DE).

Universities:
- Konstanz (DE);
- UPM-IES (ES);
- Utrecht (NL).

Research institutes:
- ECN (*coordinator*, NL);
- Fraunhofer-ISE (DE);
- IMEC (BE);
- InESS-ULP/CNRS (FR).

2 INTRODUCTION

Substantial reduction of the costs of electricity generation is crucial for photovoltaic solar energy to be able to play a substantial role in the global energy supply. The competitive position of PV and thus, the cost reduction required, varies strongly with the type of application (e.g. stand-alone rural, grid-connected roof-top or power plant), but it is generally acknowledged that a reduction to the level of retail electricity prices is an important first milestone. The latter situation is generally referred to as 'grid parity'. In a recent study by the EU PV Technology Platform [2, 3] it is shown that this would require the costs [4] of turn-key photovoltaic systems to be reduced to approximately 2 €/Wp, for typical 2007 retail electricity prices. Assuming equal shares for the modules and the Balance-of-System (BoS) in the total system costs, the costs of solar modules thus need to be reduced to 1 €/Wp or less to reach grid parity (in Southern Europe). Clearly, if retail electricity prices continue to increase as they have recently, grid parity will be reached at higher PV system costs. As a consequence, grid parity may then be reached sooner than expected (the current targets are to reach grid parity in Southern Europe by 2015 and in most of Europe by 2020).

The considerations given above are meant to put the CrystalClear cost target into application perspective. They show that if wafer-based crystalline silicon modules can be manufactured at 1 €/Wp or less, the corresponding systems may comply with the conditions for grid parity.

This paper describes the results of cost calculations for advanced wafer-based crystalline silicon modules which may be taken into production on a short or medium term. The examples analysed correspond to different technology options [5] within the category of wafer-based crystalline silicon, in particular: monocrystalline, multicrystalline and ribbon silicon as well as thin-film wafer-equivalents and front-to-rear and all-rear [6] contact and interconnection schemes.

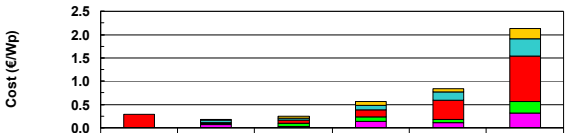
3 COST CALCULATION APPROACH

The reduction of the manufacturing costs of photovoltaic modules, like other products, is dependent on two main factors: technology improvements and effects of learning and increasing volume. In a learning curve, also referred to as price-experience curve, historic market prices are plotted as a function of the cumulatively produced volume of a specific product category, such as (crystalline silicon) solar modules [7, 8]. A learning curve thus describes the combined effects of technical innovations and volume on prices in a phenomenological way. Although a learning curve might be extrapolated to estimate the future price development in a 'top-down' manner, this is considered an approach with many uncertainties and in any case unsuitable for specific technology options within the broader category of crystalline silicon solar modules. Moreover, since learning curves relate to *prices*, translation to costs would require additional assumptions or information. Therefore we have adopted a 'bottom-up' approach in which the future manufacturing costs of solar modules are calculated based on quantifiable improvements of existing technologies and manufacturing practices [9]. The starting point of this is to describe and analyse a reference technology. This technology corresponds to the typical state-of-the-art among CrystalClear industry partners at the end of 2005 and is termed 'Basepower'. The analysis of the manufacturing costs of this reference technology has been done using cost structure data provided by the project partners. Since the 'raw' data corresponded to different production levels, they have been extrapolated to obtain a set representative for a production level in the range of 30-50 MWp per year. These corrected data have then been averaged to describe the reference technology. It is noted that only a few industry partners are active on the whole value chain from silicon crystallization and wafering to module assembly. Therefore some partners provided data on all aspects, while others gave input on specific parts only. It is emphasised that although the resulting cost structure of 'Basepower' may be typical for manufacturing practices at the end of 2005, it does *not* represent the cost structure of any of the individual project partners.

Silicon feedstock production is not a subject within CrystalClear (although studies of impurity effects and feedstock specifications are), therefore cost and performance data on silicon feedstock are treated as external input parameters.

4 COST STRUCTURE OF 2005 REFERENCE TECHNOLOGY ('BASEPOWER')

'Basepower' is a technology based on multicrystalline silicon wafers with a size 156 x 156 mm^2 and a thickness of 220 µm. The cell design features a silicon nitride front coating, an aluminium back-surface field and screen printed front and rear electrodes. Modules are manufactured using soldering for interconnection of cells with 'tabs' and foil lamination. The encapsulated cell efficiency is 14.5%. The corresponding specific silicon consumption is 9.1 g per Wp of module power.



	Feedstock	Ingot Growth	Wafering	Cell processing	Module Assembly	Total
Equipment		0.03	0.03	0.09	0.07	0.22
Labour		0.03	0.05	0.11	0.17	0.36
Material	0.29	0.04	0.08	0.15	0.42	0.99
Yield losses		0.02	0.06	0.09	0.06	0.23
Fixed		0.06	0.02	0.13	0.11	0.33
Total	0.29	0.18	0.24	0.58	0.84	2.13

Figure 1. Cost structure of the "Basepower' technology (see text), used as reference for quantification of cost reductions. Calculations are done assuming a production volume of 30-50 MWp/a.

Figure 1 gives the breakdown of direct module manufacturing costs of the 'Basepower' technology, both along the value chain (from feedstock to module assembly) and along the different cost categories (equipment, labour, etc.). The total manufacturing costs

are 2.1 €/Wp.

5 COST REDUCTION

In CrystalClear, reduction of manufacturing costs compared to 'Basepower' is pursued in two main ways:

- by developing advanced cell and module concepts with enhanced efficiency and reduced materials consumption, optimized for high-throughput manufacturing;
- by developing high-throughput, high-yield processes.

Figure 2 again shows the cost structure of 'Basepower', now divided into the shares 'silicon', 'cell processing' and 'module assembly', together with the main approaches to reduce these respective shares.

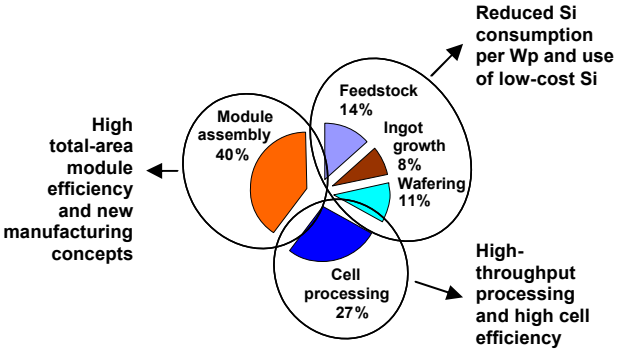


Figure 2. Relative cost structure of the "Basepower' technology (see text), with the main approaches to cost reduction.

The general approaches towards cost reduction shown in Figure 2 have been translated into a set of distinct overall (i.e. from feedstock to module) technologies by roadmapping [5, 10], see Figure 3. In the figure such an overall technology is shown as a combination of green options for processing steps as well as materials and device concepts. Selection of the options along the value chain is done based on the following main criteria:

- the overall technology should comply with the cost and environmental targets of the project (determined by cost calculations and Life Cycle Analyses (LCA));
- the technology should be of potential commercial interest for the industry partners in the consortium;
- the knowledge and research infrastructure needed to develop the technology should match the strengths of the research partners in the consortium.

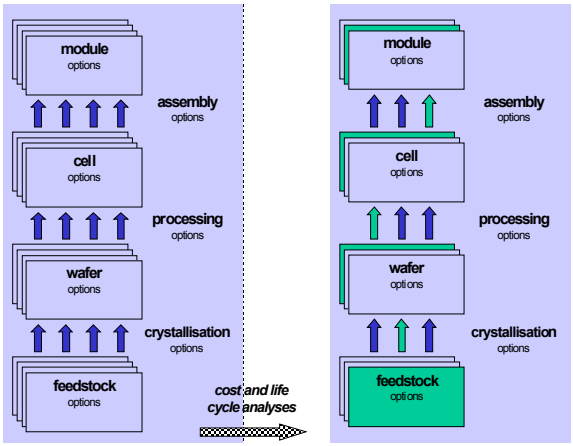


Figure 3. Construction of overall (feedstock to module) technologies by selection of options along the value chain based on cost and life cycle analyses.

The technologies selected within CrystalClear are:

1. multicrystalline silicon using front-to-rear interconnection – 'Multistar';
2. multicrystalline silicon using rear-to-rear interconnection (Metallisation-Wrap-Through, MWT) – 'MultistaR';
3. Cz monocrystalline silicon using front-to-rear interconnection – 'Superslice';
4. Cz monocrystalline silicon using rear-to-rear interconnection (Emitter-Wrap-Through, EWT) – 'SuperslicE';
5. ribbon (multicrystalline) silicon using rear-to-rear interconnection (Metallisation-Wrap-Through, MWT) – 'Ribbonchamp';
6. thin-film silicon on a low-cost substrate (so called 'wafer-equivalent') using front-to-rear interconnection – 'Epi.C'.

It is noted that all wafer technologies (1 to 5) are based on the use of very thin wafers (typically 120 µm). This necessitates the use of low-stress interconnection methods using advanced soldering techniques or conductive adhesives. In the case of MWT and EWT cells, (rear-to-rear) interconnection is done using either 'smart tabs' (specially designed metal strips) or a foil with integrated conductive pattern. The target cell efficiencies, which have also been used in the cost calculations, are 19% for monocrystalline silicon, 17% for multicrystalline silicon, and 16% for ribbon and wafer equivalent silicon (rounded numbers).

In addition to a high efficiency also a high process yield is essential to arrive at low manufacturing costs. Because it is impossible to determine the process yield in an accurate way in a research phase, we have assumed values that are considered realistic and achievable for the specific processes, materials and device concepts used.

Within the timeframe of the project, only technologies 1 to 3 will actually be developed to the level of a complete demonstrator module. Technologies 4 to 6 are described primarily as calculation examples, since development to the level of full-size modules requires

research after and beyond CrystalClear.

6 RESULTS OF COST CALCULATIONS

The technologies outlined in the previous section have been analysed in terms of direct manufacturing costs, as explained in section 3. Calculations have been done for small scale production (30 ~ 50 MWp/yr) and for large scale production (0.3 ~ 1 GWp). The economies of scale that are achieved in the latter case are presented as ranges, corresponding to the uncertainties in the assumptions, see Table I [9].

The effects of technology development (different kind and number of process steps, different kind and amount of materials consumption, higher efficiency, etc.) on costs have been quantified using detailed information provided by the research groups and their partners. Since this information is based on laboratory experience and current insights it contains inherent uncertainties. In other words, commercial manufacturing may turn out to be (or may have to be) different from what is expected. Also the costs related to the use of new materials may be different than currently foreseen. In general, we have used conservative estimates in all cases where clear uncertainties exist, meaning that our cost calculations give upper values. Moreover, we anticipate that we will update our cost calculations before the end of the project, implementing the latest insights and results. Therefore the results presented in this paper should be regarded as indicative only.

The cost of silicon feedstock is an external input parameter in the calculations and has been set at 25 €/kg for the solar grade material used in technologies 1, 2 and 5. Note that the development of specifications for solar grade silicon is an important topic in CrystalClear. This is done to be able to define the quality of silicon that yields the best price/performance ratio on module level. For the near semiconductor grade material used in technologies 3 and 4 a cost of 40 €/kg has been assumed. These values are considered realistic in a situation where feedstock supply shortages have been resolved (as expected to occur in the near future). An analysis of the impact of silicon feedstock cost on module manufacturing costs has also been made but will be reported elsewhere [11]. The cost of low grade silicon used as substrate for wafer equivalents (technology 6) is assumed to be 1.5 €/kg.

Table I. Relative economies of scale in the different cost components, for very large scale production compared to small scale production. Ranges refer to typical uncertainties. See text for further details.

	INGOT	WAFER	CELL	MODULE
Equipment	-20%/-30%			
Labour	-30%/-40%			
Materials & consumables	Crucible: -30%/-40% Other: -10%/-20%	-10%/-20%	Pastes: -30%/-40% Other: -10%/-20%	-10%/-20%
Yield	+1%/+2% (abs)	+0.5%/+1.5 % (abs)	+1%/+2% (abs)	+0.5/+1.5% (abs)
Fixed costs	-40%/-50%			

The effects of production scale as shown in Table I have been estimated using the basic principles outlined in [12]. Although this report deals with thin-film photovoltaics, it contains valuable starting points for wafer-based photovoltaics as well. It is noted that we have assumed quite modest economies of scale for wafer-based photovoltaics compared to thin-film photovoltaics. Our calculations are therefore considered to give an upper limit of costs for very large scale manufacturing. In short, when moving from small scale to very large scale production the following reduction are obtained: 20-30% for equipment costs, 30-40% for labour costs, 20-30% reduction for materials and consumables costs (typical numbers) and 40-50% for fixed costs.

Table II. Direct module manufacturing costs for large scale production. See text for details. Double numbers reflect the typical uncertainty range in the economies of volume. In *italic* the specific silicon consumption in grams per Wp of module power. *Note that all numbers are subject to change in a continuous process of updating, taking into account new insights and information as well as new research results.*

	Basepower		Multistar		MultistaR		Superslice		SuperslicE		Ribbonchamp		Epi.C	
Feedstock	0.29		0.09		0.09		0.13		0.13		0.04		0.14 (incl. layer deposition)	
Ingot growth	0.14	0.12	0.07	0.06	0.07	0.06	0.11	0.09	0.11	0.09	-		0.05	0.05
Wafering	0.20	0.18	0.11	0.10	0.11	0.10	0.10	0.09	0.10	0.09	0.09	0.08	0.08	0.07
Cell process	0.41	0.35	0.35	0.30	0.43	0.36	0.37	0.31	0.44	0.37	0.49	0.35	0.35	0.30
Module	0.67	0.58	0.52	0.45	0.52	0.45	0.47	0.40	0.54	0.47	0.69	0.53	0.53	0.46
Total €/Wp	**1.69**	**1.50**	**1.14**	**1.00**	**1.21**	**1.05**	**1.18**	**1.03**	**1.32**	**1.15**	**1.30**	**1.02**	**1.15**	**1.01**
g/Wp Si	*8.8*	*8.5*	*4.7*	*4.5*	*4.7*	*4.5*	*4.2*	*4.0*	*4.2*	*4.1*	*1.8*	*1.7*	-	-

The cost figures in Table II show the c*ombined effects* of technology development and economies of

scale. By comparing the total cost figures for 'Basepower' (the 2005 reference technology) with the other technologies it becomes clear that the reduction obtained by technology development is roughly 0.5 €/Wp, while economies of scale add another 0.5 €/Wp to that, bringing manufacturing costs down from 2.1 €/Wp for Basepower at small production scale to 1.0 – 1.3 €/Wp for new technologies at large production volumes.

Although we have separated the effects of technology development and economies of scale in the cost calculations, they are actually quite closely interlinked. The reason for this is that many of the manufacturing processes and design concepts used for the new technologies have been especially selected to enable or facilitate high-throughput (large scale) production at a high yield.

Finally we would like to point out that the manufacturing cost (or rather: the price) per Wp of module power is not the only factor determining the costs of electricity generation by PV. The latter is, among other factors, determined by the turn-key price of PV *systems*, which is the sum of module price and Balance-of-System price. The BoS contains an area-related part and a power-related part. For a given system peak power, the area-related part scales inversely with module efficiency. Therefore, modules with higher efficiency may have a somewhat higher price to yield the same economics on a system level. For this reason the EU PV Technology Platform gives a cost target range of roughly 0.2 €/Wp for modules of different efficiencies, see [2].

7 CONCLUSIONS AND OUTLOOK

CrystalClear aims at developing wafer-based crystalline silicon module technologies that can be produced at 1 €/Wp in next-generation (i.e. large) plants. The calculations described in this paper show that the costs of the technologies under development in the project consortium fall in the range of 1.0 to 1.3 €/Wp, according to current insights and information (the range results from differences *between* technologies as well as from uncertainties *per* technology). The technologies that are expected to be ready for demonstration at the full-size module level by the end of the project (mid 2009) fall in the range of 1.0 to 1.2 €/Wp. This shows that the project may reach its main target. It also demonstrates that wafer-based crystalline silicon PV is a candidate to (at least) reach grid parity on the level of retail electricity prices [2, 3].

The development of wafer-based crystalline-silicon module technology will not stop at the end of CrystalClear. There is clear and substantial potential for further improvement, beyond the performance and cost levels discussed in this paper, see also [5]. The main issues to be addressed in this context are:

- further reduction of materials costs;
- further process simplification and integration;
- optimising economies of scale;
- maintaining or increasing efficiencies under the above conditions.

It is therefore expected that wafer-based crystalline silicon will remain part of the PV technology portfolio for a long time to come.

8 ACKNOWLEDGEMENTS

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[4] The term 'cost' is to be distinguished from 'price'. For the private owner if a PV system the *costs* of electricity production would be determined by, among several other factors, the turn-key *price* paid for his or her system. As outlined in [2], reaching grid parity in Southern Europe requires turn-key system *prices* to be 2.5 €/Wp or less. Assuming a modest profit margin this would then correspond to turn-key system *costs* of less than 2 €/Wp.

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