COMPARISON OF HIGH EFFICIENCY SOLAR CELLS ON LARGE AREA N-TYPE AND P-TYPE SILICON WAFERS WITH SCREEN-PRINTED ALUMINUM-ALLOYED REAR JUNCTION

D.S. Saynova, V.D. Mihaiiletchi, L.J. Geerligs, and A.W. Weeber
ECN Solar Energy, PO Box 1, 1755 ZG Petten, The Netherlands

ABSTRACT

Low-cost, high-efficiency, and large area n-type silicon cells can be processed based on the screen printed Aluminum-alloyed rear junction concept. This process uses fabrication techniques which are very close to the current industry-standard screen printed mc-Si cell process. We compare, by experimental tests and modeling, the differences of using n-type wafers and p-type wafers with this process. An independently confirmed record-high efficiency of 17.4% is achieved on n-type floatzone (FZ) silicon wafers (area 140 cm²). On p-type FZ wafers, with the same process 17.6% is obtained, and 16.8% on p-type Cz wafers. Model calculations allow us to identify the potential for further enhancement of the n-type cell efficiency to slightly above 18.0% by improving front surface passivation. We also discuss experimental characteristics of cells produced by this process from n-type multicrystalline wafers.

INTRODUCTION

The vast majority of today's commercial silicon solar cells are made from p-type doped material. More than 80% of the produced solar cells have a homogeneous emitter, a PECVD-SiN layer as antireflective coating, and screen printed contacts on both sides. For the backside, an aluminum paste is used to create a back surface field during the contact co-firing. Recently, n-type silicon materials have received much interest as they are considered promising candidates for future generations of high-efficiency solar cells.

However, in spite of these advantages, the n-type solar cells are not yet abundantly produced in industry. In order to realize this, n-type silicon solar cells must have stable efficiencies of at least the same level as for p-type.

A few solar cell concepts based on n-type Si materials are currently under investigation. One of these concepts, investigated in this paper, is the Al-alloyed back-junction cell [3-10]. This concept was introduced for the first time by EBARA Solar Inc. in 2000 [9]. Cell efficiencies up to 17.0% were reported [7]. It represents a fast way, for industry, to move from p-type to n-type substrates because of the possibility of maintaining the same process sequence. The only difference, compared with the conventional p-type (n’pp’) process used in industry for p-type wafers, is that during the phosphorus diffusion a front surface field is created instead of an emitter, and during the contact co-firing the aluminum back junction is formed.

Aluminum rear-junction cells are also an interesting and simple approach to study and identify the material limitations for all back-contacted solar cells, in particular, for multicrystalline n-type substrates.

In this paper we present results on our n-type cell development based on the Al back-junction. We compare by experimental tests and modeling the differences of using n-type wafers versus p-type wafers, applying the same processing sequence. We present an independently confirmed record-high efficiency of 17.4% based on n-type float zone (FZ) wafers, which demonstrates the potential for high efficiency of this n-type process. On p-type FZ wafers with the same process 17.6% was obtained, whereas 16.8% was obtained on p-type Cz wafers.

EXPERIMENTAL PROCEDURE

The cell process was mainly focussed on 148.5 cm² n-type and p-type monocrystalline silicon wafers, but results on 156.25 cm² industrial n-type multicrystalline silicon (mc-Si) wafers are also presented in this paper. The cell process we used is based on in-line processing for diffusion, co-firing, and on process steps which can be industrialized. It starts by a texture etch (industrial isotexture, or random pyramids) of the surface. Then the front-surface field (n-type wafer) or front emitter (p-type wafer) is formed by phosphorus diffusion in an infrared conveyor belt furnace from a spin-on source. To improve the accuracy of our modeling, and investigate the potential improvements in cell efficiency by improvement of the front properties, two front diffusions were tested: one standard diffusion (~60 Ohm/sq) and one diffusion for improved front surface properties. Subsequently, a rear side polishing etch is carried out followed by the phosphorus glass removal and the PECVD SiNₐ anti-reflection coating deposition on the front side. This process sequence does not further require wafer dicing or other methods for junction isolation, and thus the entire initial wafer area is used. The silver grid is then screen-printed on the SiNₐ front side, followed by screen-printing of Al on the whole rear side of the cell. Both contacts are co-fired in an infrared conveyor belt furnace, thus forming also the p⁺ emitter (n-type wafer) or BSF (p-type wafer) at the rear. The process flow chart and a schematic cross section of the Al back junction solar cell are shown in Fig. 1.

CELL PROCESS AND RESULTS

Effect of base resistivity and front diffusion

Table 1 summarizes solar cell parameters obtained for
n-type mc-Si and FZ substrates of different base resistivities, and for the two different front diffusions. It is observed that the highest n-type cell efficiency is obtained for high substrate resistivity. This is in agreement with model calculations [4,8], which show that, in order to benefit from the full potential of this type of solar cell, the wafer resistivity should typically be higher than 10 Ωcm. The IQE fit of the 6.0(±1) ms, and does not limit the IQE. The fit to experimental data reveals a SRV of 6.0(±1)×10^5 cm/s independent of the base resistivity.

The bulk lifetime must be taken into account, however, for multicrystalline wafers. The IQE fit of the multicrystalline cell with base resistivity 0.8 Ωcm from Table 1 reveals the same SRV value as that obtained for the monocristalline cells above (6.0×10^5 cm/s), but with a considerable lower bulk lifetime of only 28 µs (as obtained from PC1D fit). The ratio of diffusion length and substrate thickness (L_d/W) must be higher than 2.5 for good cell performance [11]. To meet these conditions, the effective lifetime of the multicrystalline substrates must be higher than 130 µs. Fortunately, resistivity and bulk lifetime usually go together: increasing bulk resistivity also increases the bulk lifetime.

<table>
<thead>
<tr>
<th>wafer</th>
<th>ρ [Ωcm]</th>
<th>J_sc [mA/cm^2]</th>
<th>Voc [mV]</th>
<th>FF [%]</th>
<th>η [%]</th>
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<td>mc</td>
<td>0.8</td>
<td>19.77</td>
<td>589</td>
<td>73.7</td>
<td>8.6</td>
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<tr>
<td>mc</td>
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<td>29.7</td>
<td>580</td>
<td>72.1</td>
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<td>FZ</td>
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<td>77.9</td>
<td>14.9</td>
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<td>± 1</td>
<td>±0.6</td>
<td>±0.1</td>
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<tr>
<td>FZ best</td>
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<td>34.75</td>
<td>626</td>
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<tr>
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<td>623</td>
<td>76.8</td>
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</tr>
<tr>
<td>average</td>
<td>± 0.06</td>
<td>± 3</td>
<td>±0.4</td>
<td>±0.2</td>
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</table>

Table 1. Effect of base resistivity (ρ) and front diffusion on n-type FZ and mc-Si cell properties. All cell surfaces are isotextured. Above dashed line: standard front diffusion. Below dashed line: optimised front diffusion. The area of the solar cells is 156.25 cm^2 for mc-Si cells and 148.5 cm^2 for monocrystalline cells.

Lowering the front surface recombination velocity

Currently we are investigating ways to reduce the SRV of these types of cells and, thus, to further improve their efficiency. In the lower part of Table 1 (below dashed line) the results for an improved phosphorus diffusion are shown. It is observed that a higher J_sc is achieved by engineering the FSF diffusion and improving the cell...
process. In other experiments we also observed improvements in $V_{oc}$ up to 12 mV due to the improved front diffusion [12]. However, the $V_{oc}$ results show more scatter.

As a result of the new process, the SRV was further reduced to $8.5 \pm 1.5 \times 10^4$ cm/s (determined by fitting the IQE data). Model calculations [12] indicate that the gain in $J_{sc}$ and $V_{oc}$ of the cells is indeed due to a lower SRV.

**Best cell efficiencies for p-type and n-type substrates**

The best cell results are obtained using a random pyramids texture etched surface and the optimized diffusion. The conversion efficiencies that we reached on n-type FZ wafers are 17.3% on 148.5 cm$^2$, and 17.4% on 140 cm$^2$ (after dicing away the unprinted Al area on the rear side), independently confirmed at Fraunhofer ISE CalLab, Freiburg, Germany. To our knowledge, this is the highest efficiency obtained for n-type silicon solar cells featuring a screen-printed aluminum rear-emitter.

Table 2 shows best results for n-type cells, as well as for p-type cells processed in the same way. Clearly, for the diffusion parameters used, the results on the two types of FZ wafers do not differ much. However, compared to p-type Cz wafers the n-type process performs better. It is expected that n-type Cz wafers will perform as well as the n-type FZ wafers (n-type Cz wafers of appropriate resistivity were not available for tests). The $V_{oc}$ of 633 mV for the n-type FZ cells is among the highest measured on large area (148.5 cm$^2$) solar cells featuring screen printed contacts and is already close to the $V_{oc}$ limit (about 642 mV) of an Al-alloyed rear full area emitter cell [10, 13].

Table 2: Parameters of the best fabricated solar cells on FZ and mc-Si substrates. The area of the solar cells is as in Table 1. ST - surface texture.

<table>
<thead>
<tr>
<th>Si</th>
<th>ST</th>
<th>$\rho$ [\Omega cm]</th>
<th>$J_{sc}$ [mA/cm$^2$]</th>
<th>$V_{oc}$ [mV]</th>
<th>FF [%]</th>
<th>$\eta$ [%]</th>
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<td>582</td>
<td>74.5</td>
<td>13.6</td>
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<tr>
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<td>IS</td>
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<td>33.5</td>
<td>603</td>
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<td>15.5</td>
</tr>
<tr>
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<td>IS</td>
<td>31</td>
<td>33.27</td>
<td>633</td>
<td>78.8</td>
<td>16.6</td>
</tr>
<tr>
<td>n-FZ</td>
<td>RP</td>
<td>31</td>
<td>35.53</td>
<td>632</td>
<td>77.4</td>
<td>17.4</td>
</tr>
<tr>
<td>p-FZ</td>
<td>RP</td>
<td>2.4</td>
<td>35.52</td>
<td>626</td>
<td>79.0</td>
<td>17.6</td>
</tr>
<tr>
<td>p-Cz</td>
<td>RP</td>
<td>1.1</td>
<td>35.76</td>
<td>617</td>
<td>76.0</td>
<td>16.8</td>
</tr>
</tbody>
</table>

It is clear that for n-type mc-Si wafers, it is difficult to obtain sufficient performance. In the comparison of the mc-Si cells in Table 2 it should also be noted that the p-mc-Si cells were processed on wafers from the upper part of an ingot, which results in some reduction of cell efficiency due to increased crystal defect density.

**Fig. 3. Internal quantum efficiency (IQE) data of the best monocrystalline p-type and n-type solar cells.**

**Fig. 4. Calculated solar cell efficiency as a function of surface recombination velocity for an n-type FZ with a resistivity of 30 $\Omega$cm. The calculation is done considering a FF of 78.8% and a random pyramid texture surface. The parameters used in the calculation are those found by fitting the experimental data of Figure 2.**

**Potential of n-type FSF cell process**

In Fig. 4 a model calculation for the conversion efficiency versus SRV is shown. The starting point of this calculation was the experimental data of the 17.4% efficiency cell. It is clear from the figure that efficiencies only slightly over 18% can be obtained even after fully minimizing SRV. With the FF reaching 79% there are two major factors left that limit the efficiency of this industrial screen-printed aluminium rear-emitter cell: Firstly, the metallization shading of the front surface (which amounts to 7.5% in our cells), and, secondly, the fundamental limitation imposed on $V_{oc}$ (and $J_{sc}$), of approximately 642 mV, due to recombination that occurs in the Al-alloyed emitter.

Cuevas et al. [10] have reported that the recombination current density in the p$^+$ region formed by screen printed aluminium and alloying cannot be lower...
than approximately $5 \times 10^{-10}$ mA/cm$^2$. Such recombination can drastically limit the $J_{sc}$ and $V_{oc}$ of a cell even if front SRV is minimized and high quality wafers are used [10, 13]. Recently Bock et al. [14] reached 250 fA/cm$^2$ using low temperature annealed a-Si as surface passivation layer on the rear aluminum-doped emitter, after etching away the metallic aluminum layer. Preliminary modeling shows this could increase the cell efficiency by about 0.2%.

**n-type mc-Si substrates**

As Fig. 5 shows, the n-type mc-Si cells are strongly limited by the poor performance at crystal defects for short and middle wavelengths, which the slightly better performance at long wavelengths (compared to p-type wafers) cannot compensate for. From the cell results in Table 2, it seems that in n-type mc-Si cells especially the $V_{oc}$ is suppressed. In addition, the n-type mc-Si wafers that we have used originate from the edge of an ingot (top edge in Fig. 5) which also reduces performance.

![Fig. 5. Local light beam induced current data of the p-type (top) and n-type (bottom) mc-Si solar cells from Table 2. Light is 404nm wavelength. Bottom right insets in both images: light of 976nm. Same scale in both figures.](image)

The best efficiency we obtained so far is 13.6%, while Kopecek et al [8] have reported 14.4% for a wafer from the center of an ingot. It is known that 130 µs lifetime, which is good enough to reach high efficiencies on homogeneous substrates, can be obtained quite well in n-type mc-Si. The main issue is, however, to produce sufficiently homogeneous mc-Si.

**CONCLUSIONS**

We have demonstrated that a low cost process of fabricating n-type solar cells based on the Aluminum rear-emitter concept leads to a new record efficiency of 17.4% for large area monocrystalline FZ substrates. The same process on p-type monocrystalline substrates resulted in 17.6% (FZ) and 16.8% (Cz) efficiency. By improving the front surface passivation somewhat higher efficiencies can still be realized on n-type wafers with this process, but the results are already quite close to fundamental limitations due to the rear Al emitter. High efficiencies may also be conceivable on n-type multicrystalline substrates if those can be produced with high lifetime and, especially, high homogeneity.

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**REFERENCES**


Cells, 65, 2001, p. 621.


